What is claimed is:

1. A semiconductor memory component, comprising:

a first memory cell transistor electrically connected to a first selection line;

a second memory cell transistor electrically connected to a second selection line; and

a first row-select/potential-equalization line and a second row-select/potential-equalization line, wherein the two row-select/potential-equalization lines are arranged vertically one above the other and between the two memory cell transistors.

2. The semiconductor memory component of Claim 1, wherein at least one of the two line select/potential equalization lines is equidistance from the first and the second memory cell transistors.

3. The semiconductor memory component of Claim 1, wherein at least one of the two row-select/potential-equalization lines is arranged above and centered over a diffusion region of the first and second memory cell transistors, and wherein the diffusion region is shared between the first and second memory cell transistors.

4. The semiconductor memory component of Claim 1, wherein the first and second row-select/potential-equalization lines are arranged one above the other so that they are coincident in the vertical direction.

5. The semiconductor memory component of Claim 1, wherein the two row-select/potential-equalization lines are formed in different metallization planes.

6. The semiconductor memory component of Claim 5, wherein the first row-select/potential-equalization line is formed in the second or third metallization plane, and the second row-select/potential-equalization line is formed correspondingly in the third or second metallization plane above the first and the second memory cell transistors.

7. The semiconductor memory component of Claim 1, wherein the first or the second selection line is electrically connected to the first or the second row-select/potential-equalization line, respectively.

8. The semiconductor memory component of Claim 1, further comprising a data line selectively coupled to the first and second memory transistors in a metallization plane that is above the metallization planes in which the first and the second row-select/potential-equalization line are located.

9. The semiconductor memory component of Claim 1, further comprising:

a memory cell field in which a plurality of memory cells are arranged in the form of a matrix,

wherein the measurement cell field has a first and a second row, each with a plurality of measurement cells, each cell with its own memory cell transistor, where memory cell transistors of the first row are electrically connected to the first selection line and the memory cell transistors of the second row are electrically connected to the second selection line, and

wherein the first selection line is electrically connected only to the first row-select/potential-equalization line, and the second selection line is connected only to the second row-select/potential-equalization line.

10. The semiconductor memory component of Claim 1, further comprising:

a memory cell field in which a plurality of memory cells are arranged in the form of a matrix,

wherein the memory cell field has a first and a second row, each with a plurality of memory cell transistors, where memory cell transistors of the first row are electrically connected to the first selection line and the memory cell transistors of the second row are electrically connected to the second selection line, and

wherein both the first and the second selection lines each has at least one electrical connection to the first and an electrical connection to the second row-select/potential-equalization line.

11. A process for producing a semiconductor memory component, comprising:

forming a first and second memory cell transistor in a substrate;

electrically connecting the first memory cell transistor to a first selection line, and the second memory cell transistor to a second selection line (WL2);

forming a first row-select/potential-equalization line and a second row-select/potential equalization line, wherein the first and second row-

select/potential-equalization lines are arranged vertically one above the other and between the two memory cell transistors.

12. The process of Claim 11, wherein at least one of the two row-select/potential-equalization lines is equidistant from the two memory cell transistors.

13. The process of Claim 11, wherein at least one of the two row-select/potential-equalization lines is above and centered over a diffusion region of the first and second memory cell transistors, and wherein the diffusion region is shared between the first and second memory cell transistors.

14. The process of Claim 11, wherein the first and the second row-select/potential-equalization lines are arranged one above the other so that they are coincident in the vertical direction.

15. The process of Claim 11, wherein the first and the second row-select/potential-equalization lines are formed in different metallization planes.

16. The process of Claim 11, further comprising forming a data line in a metallization plane above the memory cell transistors, wherein the data line metallization plane is formed above the metallization planes in which the row-select/potential-equalization lines are formed.

17. The process of Claim 11, further comprising:

forming a plurality of memory cells in each of a first and second row of a memory cell field designed in the form of a matrix;

wherein a memory cell transistor is formed in each memory cell and has a row-select/potential-equalization line associated therewith, and the memory cell transistors of the first row are electrically connected to a first selection line, and the memory cell transistors of the second row are electrically connected to a second selection line; and

electrically connecting the first selection line to the row-select/potential-equalization lines of the memory cell transistors in the first row, and

electrically connecting the second selection line to the row-select/potential-equalization lines of the memory cell transistors in the second row.

18. The process of Claim 17, wherein the first selection line is electrically connected to the row-select/potential-equalization lines of the second row, and the second selection line is electrically connected to the row-select/potential-equalization lines of the first row.